EE 2700 Project 1 – Arithmetic Logic Unit

This project may be done individually or in teams of two. You may consult others for general questions but do not copy schematics or test bench code. Cheating will result in a zero score for this part of the project.

1. Design a simple arithmetic logic unit (ALU) using gates and/or other logic devices. Your design should be hierarchical. The top level design should consist of interconnected components. Those components should, in turn, consist of gates and/or smaller components.

2. The inputs of the ALU are two 8-bit values (A and B), a 1-bit carry-in, and a three- or four-bit operation code (opcode). The outputs of the ALU are an 8-bit result and a 1-bit carry-out. The result and carry-out are based on the opcode and the input values according to the table below:

Opcode	Result	Carry-out
Add	A + B	1 if carry occurs, else 0
Addc	A + B + Carry-in	1 if carry occurs, else 0
Exclusive-Or	A ⊕ B	Carry in
Load	B	Carry in
Hold	A	Carry in

   Exclusive-or (xor) is a logical operation (similar to AND or OR). The truth table for exclusive-or is given below:

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

   For the ALU, exclusive-or is applied individually to each bit of the input. For example, if A = 00110101 and B = 10100110 then A ⊕ B = 10010011.

3. You are free to assign the opcodes any way that you like. Some opcode assignments will simplify your design.

4. Capture your schematics using ISE. Capture first the smaller components in your design and test/simulate them. Once you are satisfied, make schematic symbols for them and move on to larger (higher level) components. You are free to use the pre-defined components in ISE. Use busses wherever you can. In particular, the signals A, B, Result and Opcode *must* be busses in the top level schematic.

5. Write a VHDL test bench and simulate your design to verify that each opcode produces the correct result and carry-out for the following input combinations:

A (hex)	B (hex)	Carry in
00	00	1
7F	81	0
9A	65	1
6B	8F	1

6. Turn in the schematic(s), the VHDL test bench and the simulation results on or before the due date given on the course web site.

This week during your lab period, your lab instructor will be available to assist you with this project, but you should try to design your ALU and capture your schematic(s) before coming to lab.